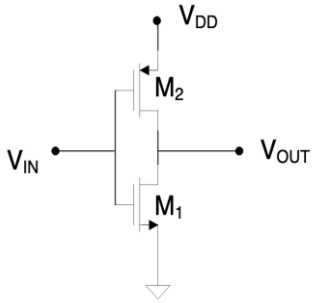
EE 3300
Homework 14
Fall 2024
Due Friday Dec 6 1:00 p.m.

Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 250\mu A/V^2$, $V_{Tn} = 0.4V$, all p-channel transistors have model parameters $\mu_p C_{OX} = \mu_n C_{OX}/3$, $V_{Tp} = -0.4V$, and $C_{OX}=4fF/u^2$. When reference is made to a reference inverter, use the same reference inverter that was introduced in the lecture notes.

Problem 1

If $\frac{W_2}{L_2} = \frac{W_1}{L_1}$, what is the trip point of the inverter? What if $\frac{W_2}{L_2} = \frac{5W_1}{L_1}$? Assume V_{DD}=3V.



Problem 2

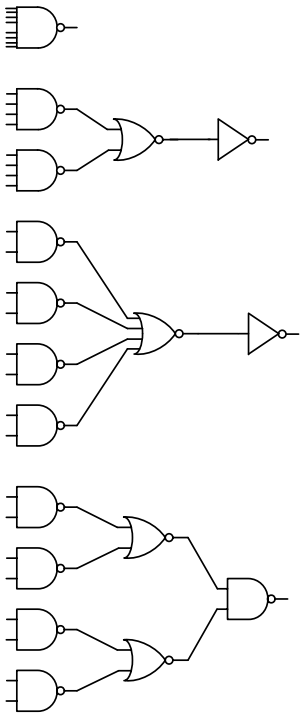
What is the propagation delay for a k-input NOR gate where all devices are minimum sized? What about a NAND gate? Assume the load capacitance is equal to C_{REF} and V_{DD}=3V.

Problem 3

Assume a load capacitance of 30fF is to be driven. Determine t_{HL} and t_{LH} if it is driven by an equal rise/fall inverter (termed the reference inverter) and if it is driven by a minimum-sized inverter.

Problem 4

Four different implementations of the 8-input NAND function are shown. If the devices are sized for equal worst-case rise and fall times, compare the input capacitance at each input and the total gate area for these 4 different implementations



Problem 5

Size the devices in a 3-input NOR gate for equal worst-case rise and fall times. Assume V_{DD}=3V.

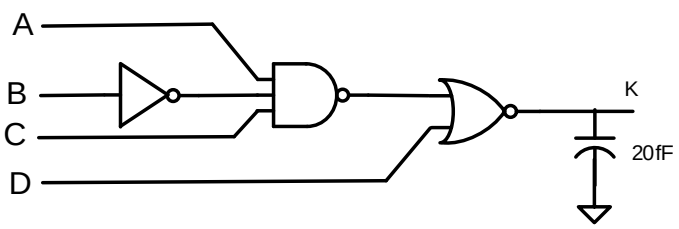
Problem 6

Consider a two-input NOR gate sized for equal worst-case rise and fall times that is driving an identical device thereby forming a two-gate cascade.

a) Determine the trip points for all combinations of input transitions
b) Determine the fastest and slowest t_{LH} for the output of the first gate in this cascade.

Problem 7

Determine the propagation delay in terms of t_{REF} from B to K for the following circuit. Assume all devices sized for equal worst-case rise and fall times (with OD=1).



Problem 8

Using Static CMOS Logic, create a circuit at the transistor level to realize the following Boolean expression. Size the devices for equal worst-case rise and fall times.

$$F = \overline{(AB + C)D}$$

Problem 9

The circuits shown have been proposed as digital inverters. Determine which will behave as digital inverters and which will not. If the circuit performs as a digital inverter, determine V_H and V_L.